IME-03-011

April 2, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/763,304 01/23/04

Shajan Mathew et al.

SALICIDE PROCESS FOR METAL GATE CMOS DEVICES

INFORMATION DISCLOSURE STATEMENT

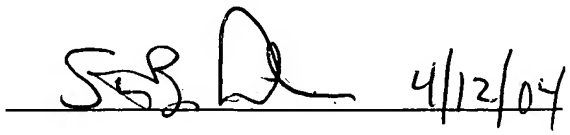
Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 12, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date  4/12/04

In "High Performace Damascene Metal Gate MOSFET's for 0.1um Regime," IEEE Trans. on Electron Devices, Vol. 47, No. 5, May 2000, pp. 1028-1034 by Yagishita et al., discuss a novel transistor formation process (damascene gate process) developed in order to apply metal gates and high dielectric constant gate insulators to MOSFET fabrication and minimize plasma damage to gate insulators.

"CMOS Metal Replacement Gate Transistors using Tantalum Pentoxide Gate Insulator," by Chatterjee et al., IEDM 98-777, 29.1.1 to 29.1.4, reports a full CMOS process uisng a combination of a TiN/W Metal Replacement Gate Transistor design with a high dielectric constant gate insulator of tantalum pentoxide over thin remote plasma nitrided gate oxide.

U.S. Patent Application Publication US 2002/0123222 A1 to Wu, "Method of Fabricating a Salicide Layer," discusses a method of fabricating a salicide layer.

U.S. Patent 6,475,874 to Xiang et al., "Damascene NiSi Metal Gate High-K Transistor," discloses a method for implementing a self-aligned low temperature metal silicide gate.

U.S. Patent 6,503,833 to Ajmera et al., "Self-Aligned Silicide (Salicide) Process for Strained Silicon MOSFET on SiGe and Structure Formed Thereby," discloses a method of forming a semiconductor substrate (and resultant structure).

U.S. Patent 6,534,390 to Chong et al., "Salicide Method for PRoducing a Semiconductor Device Using Silicon/Amorphous Silicon/Metal Structure," discloses an improved semiconductor device of a Silicon/Amorphous Silicon/Metal Structure (SASM) and a method of making an improved semiconductor device by a salicide process.

U.S. Patent 6,436,840 to Besser et al., "Metal Gate with CVD Amorphous Silicon Layer and a Barrier Layer for CMOS Devices and Method of Making with a Replacement Gate Process," discusses a semiconductor structure and method for making the same which provides a metal gate on a silicon substrate.

U.S. Patent 6,440,868 to Besser et al., "Metal Gate with CVD Amorphous Silicon Layer and Silicide for CMOS Devices and Method of Making with a Replacement Gate Process," discloses a semiconductor structure and method for making the same which provides a metal gate on a silicon substrate.

U.S. Patent 6,326,251 to Gardner et al., "Method of Making Salicidation of Source and Drain Regions with Metal Gate MOSFET," discusses a method of forming a transistor which includes forming a source/drain implant in the initial processing stages just after the formation of the isolation and active regions on the substrate.

U.S. Patent 6,084,279 to Nguyen et al., "Semiconductor Device Having a Metal Containing Layer Overlying a Gate Dielectric," discusses metal semiconductor nitride gate electrodes formed for use in a semiconductor device.

U.S. Patent 6,475,908 to Lin et al., "Dual Metal Gate Process: Metals and Their Silicides," describes methods for forming dual-metal gate CMOS transistors.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
IME-03-011	10/763,304
Applicant: Shajan Mathew et al.	
Filing Date: 01/23/04	Group Art Unit:

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	6475874	11/5/02	Xiang et al.	438	396	12/7/00
	6503833	1/7/03	Ajmera et al.	438	682	11/15/00
	6534390	3/18/03	Chang et al.	438	592	1/16/02
	6436840	8/20/02	Besser et al.	438	721	10/19/00
	6440868	8/27/02	Besser et al.	438	721	10/19/00
	6326251	12/4/01	Gardner et al.	438	197	1/12/99
	6084279	7/4/00	Nguyen et al.	257	412	3/31/97
	6475908	11/5/02	Lin et al.	438	659	10/18/01

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	
-	"High Performance Damascene Metal Gate MOSFET's for 0.1 μm Regime", IEEE Trans. on Electron Devices, Vol. 47, No. 5, May 200, pp. 1028-1034 by Yagashita et al..
-	"CMOS Metal Replacement Gate Transistors using Tantalum Pentoxide Gate Insulator" by Chatterjee et al., IEDM 98-777, 29.1.1 to 29.1.4.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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-		U.S. Patent App. Publication US 2002/0123222 A1 to Wu, Pub. Date 9/5/02, Filed 3/1/01, US Cl 438/682, "Method of Fabricating a Salicide Layer".

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